In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Canceled).

2. (Currently Amended) ~~The method of claim 1,~~ A method for reducing Critical Dimension (CD) non-uniformity in creating a patterned layer of semiconductor material, comprising:

providing a substrate, said substrate having been provided with one or more layers of semiconductor material; depositing a first masking layer over one or more layers of semiconductor material;

creating, while applying methods for compensation of optical proximity effects and micro-loading, a first pattern in said first masking layer, said first pattern being a pattern of high-density semiconductor device features and isolated semiconductor device features and dummy features, said creating while applying methods for compensation of optical proximity effects and micro-loading a first pattern in said first masking layer comprising:

first exposing said first masking layer with a first mask, said first mask comprising a first and a second pattern, said first pattern being a pattern of high-density semiconductor device features having a first cross-section, said second pattern being full-size assist features having a second cross-section, said full-size assist features being designed to maximize contribution to spatial frequency and to achieve unification of an exposure level of the high-density device features;

second exposing said first masking layer with a second mask, said second mask comprising a third pattern, said third pattern aligning with said second pattern on said first mask; and etching said first masking layer in accordance with said first and second exposure of said masking layer;

patterning at least one of said one or more layers of semiconductor material in accordance with said first pattern; removing said first masking layer;

depositing a second masking layer over said at least one layer of semiconductor material, including said patterned at least one of said one or more layers of semiconductor material;

creating a second pattern in said second masking layer, said second pattern exposing dummy features of said patterned at least one of said one or more layers of semiconductor material;

patterning said at least one layer of semiconductor material in accordance with said second pattern; and

removing said second masking layer.

3. (Original) The method of claim 2, said third pattern having dimensions being larger than dimensions of said second pattern by a measurable amount.

4. (Original) The method of claim 2, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features being within a range of between about 0.5 and 3.0 times said cross-section of said high-density semiconductor device features.

5. (Original) The method of claim 2, said first cross-section being about equal to said second cross-section.

6. (Original) The method of claim 2, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features and said isolated features and said dummy features being determined by first independent parameters, said first independent parameters being dimensions of said high-density semiconductor device features, said first independent parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

7. (Original) The method of claim 2, a design of said full-size assist feature being determined by second independent parameters, said second independent parameters being dimensions of said high-density semiconductor device features, said second independent parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

8. (Original) The method of claim 2, said first masking layer comprising photoresist.

9. (Original) The method of claim 2, said first and said second pattern comprising an opaque surface region of said first mask surrounded by a transparent background surface region.

10. (Original) The method of claim 2, said first and said second pattern comprising a transparent surface region of said first mask surrounded by an opaque background surface region.

11. (Original) The method of claim 2, said third pattern comprising an opaque surface region of said first pattern surrounded by a transparent background surface region.

12. (Original) The method of claim 2, said third pattern comprising a transparent surface region of said first pattern surrounded by an opaque background surface region.

13. (Original) The method of claim 2, said first masking layer comprising an insulating material.

14. (Original) The method of claim 2 wherein overlapping full-size assist features of said second pattern of full-size assist features are combined into larger full-size assist features.

15. (Original) The method of claim 2 wherein said second pattern comprises side-by-side full-size assist features.

16. (Original) The method of claim 2, said third pattern being aligned with said first pattern, keying said third pattern to said first pattern.

17. (Original) The method of claim 2, elements of said second pattern being interspersed with elements of said first pattern.

18. (Original) The method of claim 2, elements of said second pattern surrounding elements of said first pattern.

19. (Currently Amended) The method of claim [[1]] 2, said second masking layer comprising photoresist.

20. (Currently Amended) The method of claim [[1]] 2, said at least one layer of semiconductor material being a layer of dielectric, a layer of insulating material, a layer of passivation material, a layer of hardmask material or a layer of conductive material.

21. (Currently Amended) The method of claim [[1]] 2, said high-density semiconductor device features being separated by a distance of 2.0 μm or less.

22. (Currently Amended) The method of claim [[1]] 2, said isolated semiconductor device features being separated from adjacent pattern features by a distance of 2.0 μm or less.

23. (Currently Amended) The method of claim [[1]] 2, said dummy features being separated from adjacent high-density semiconductor device features or isolated semiconductor device by a distance of 2.0 μm or less.

24-46. (Canceled).